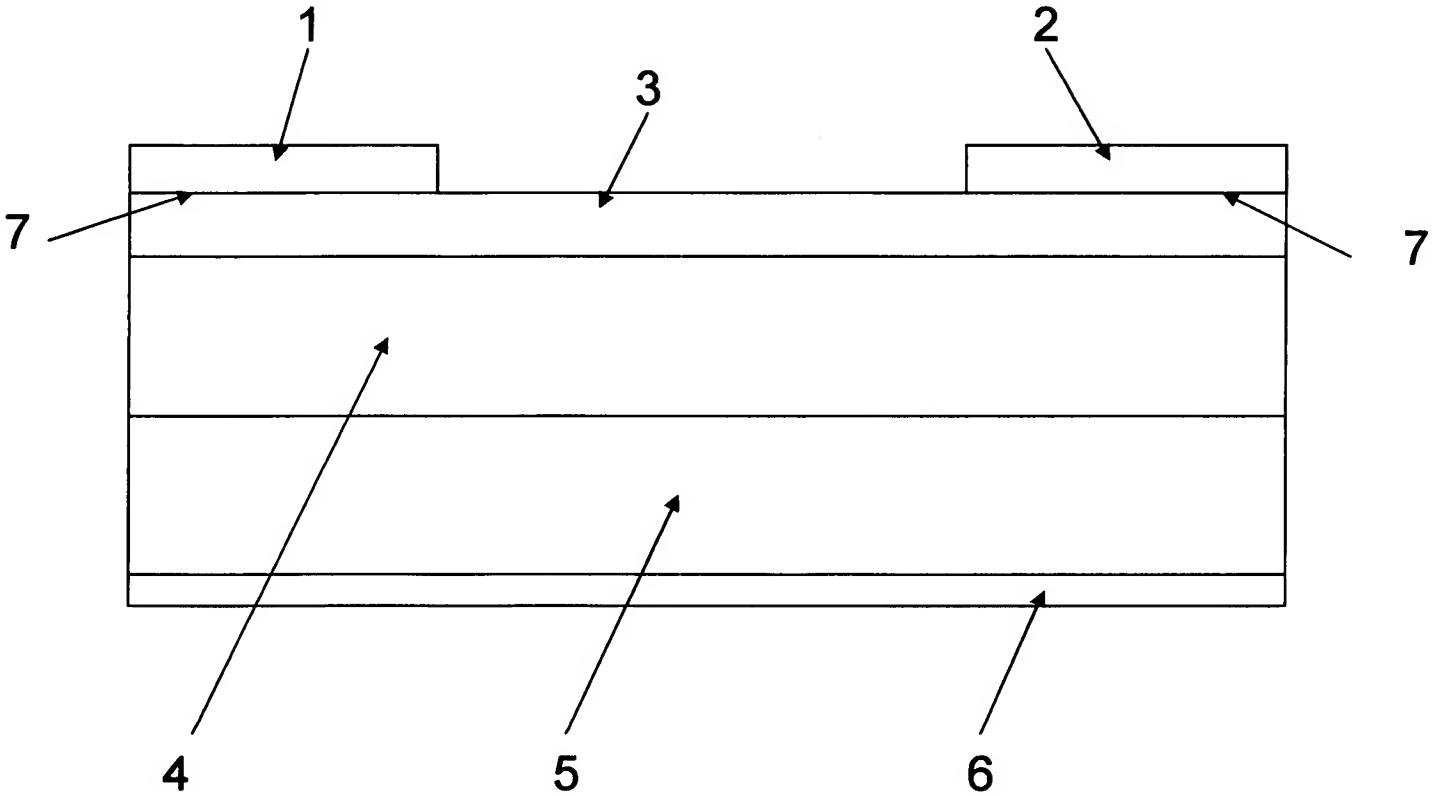
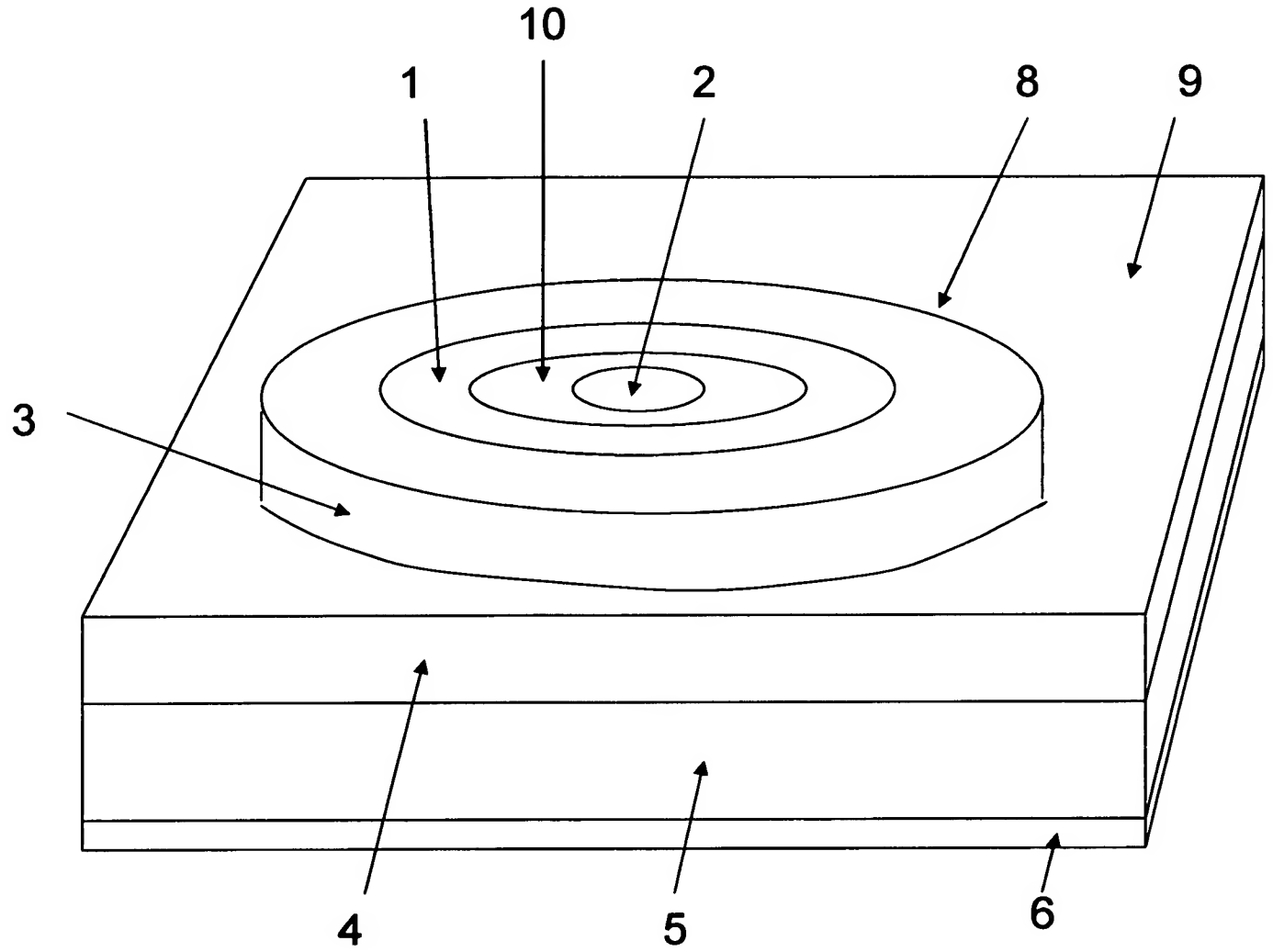


Figure 1.



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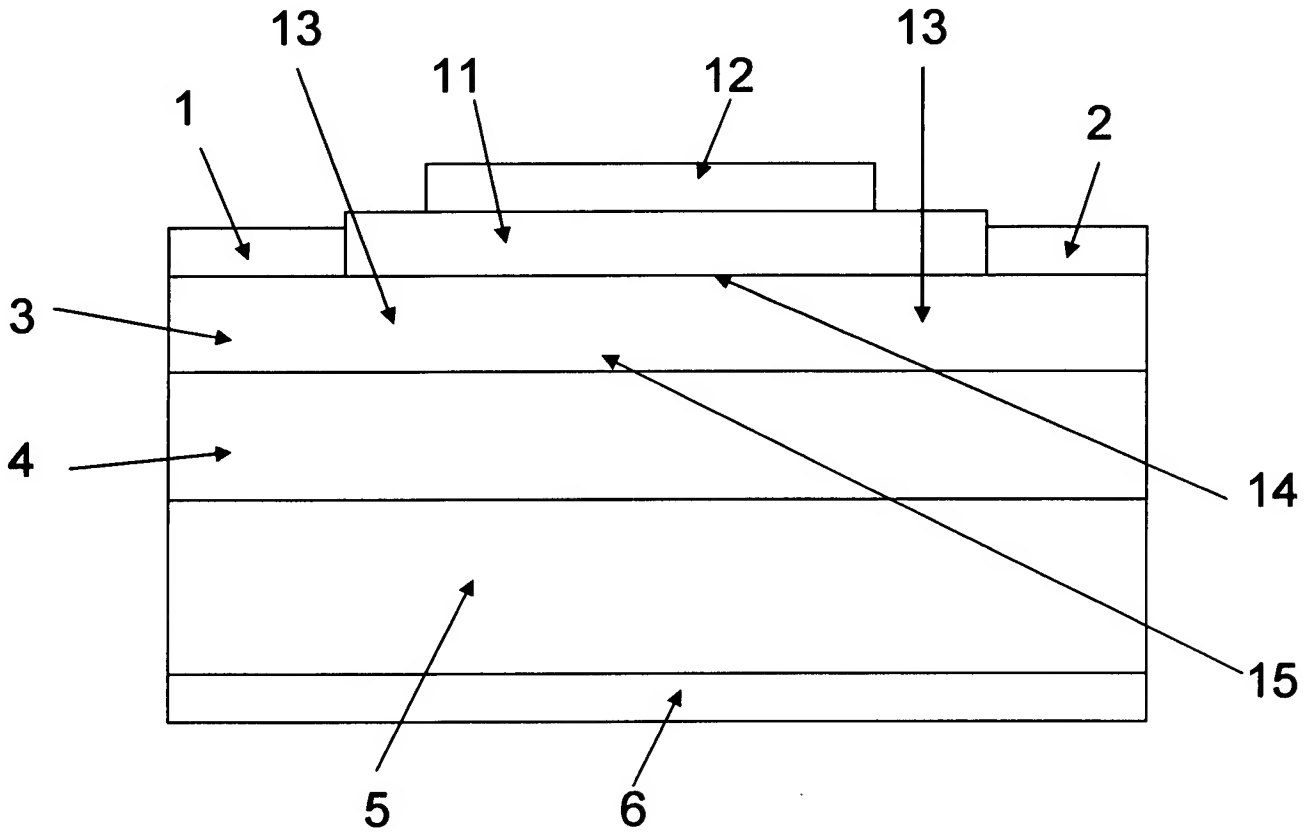

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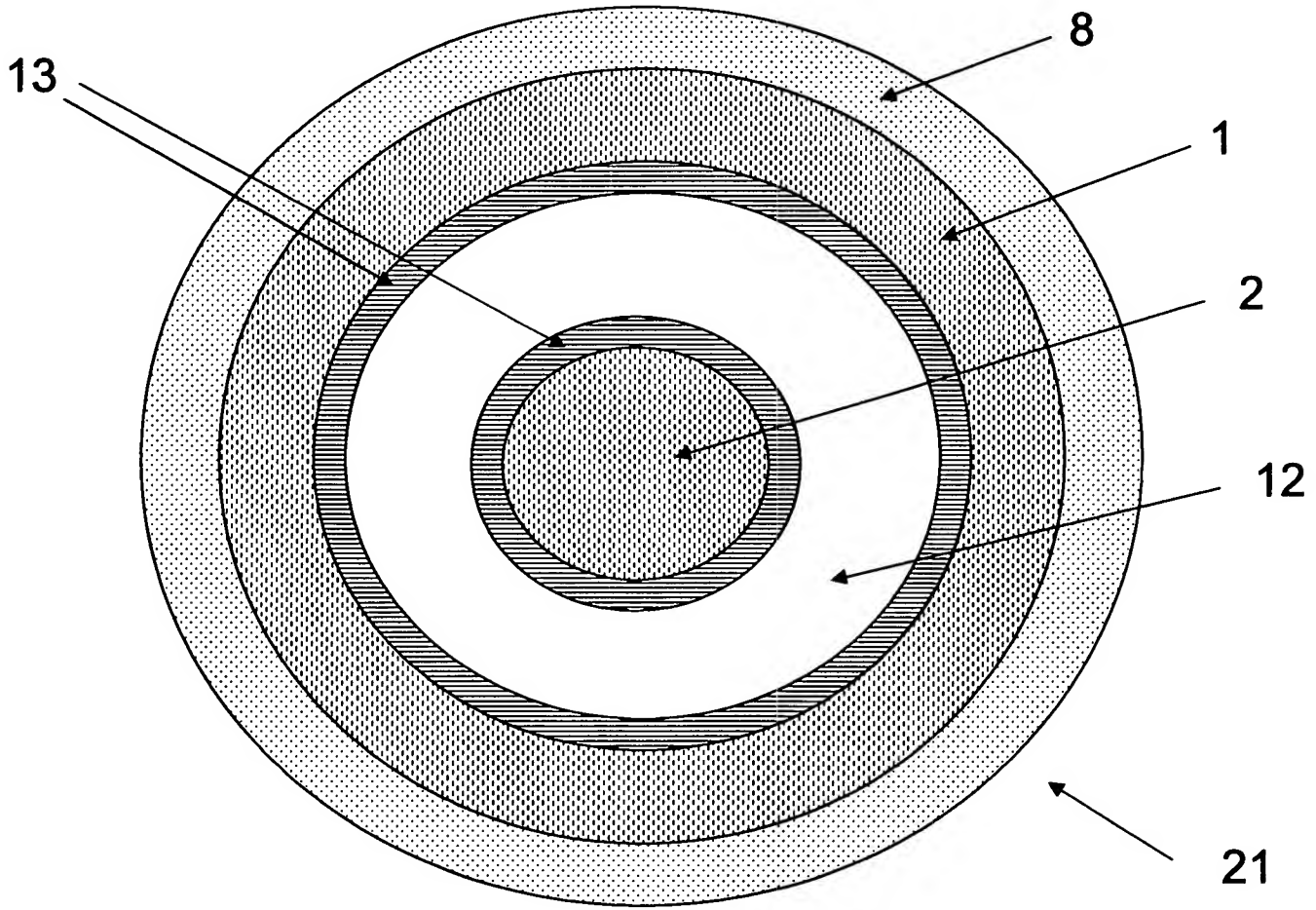

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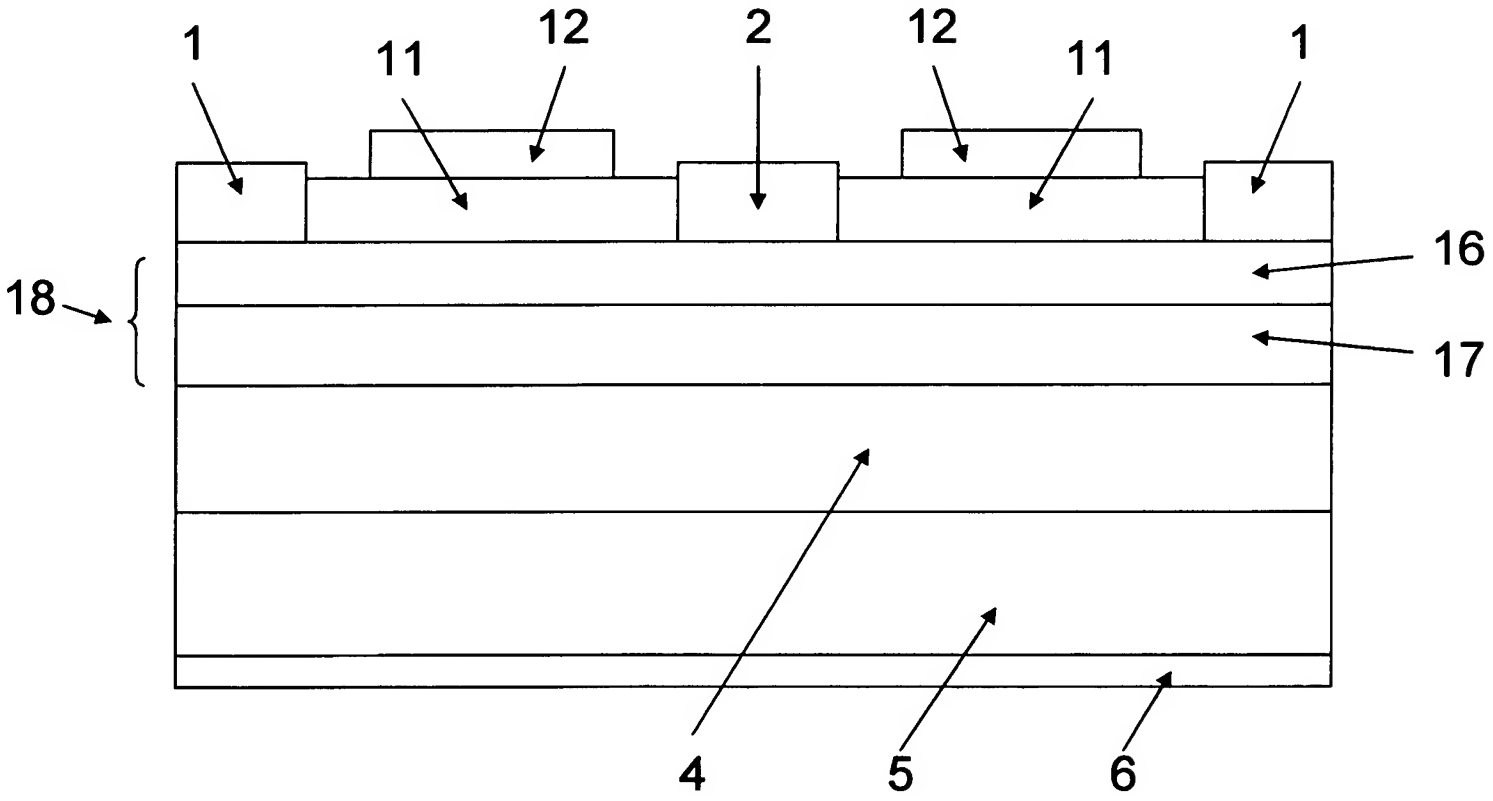

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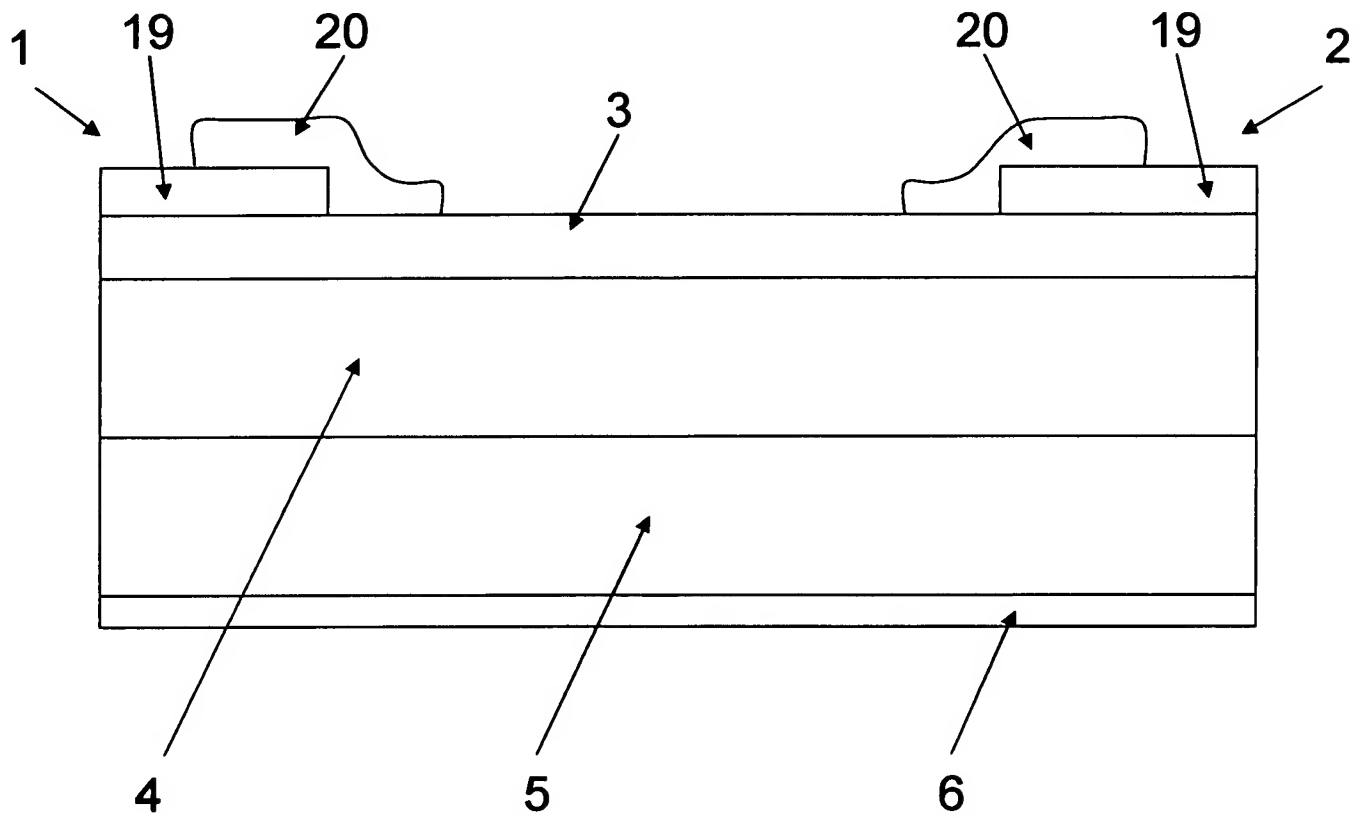

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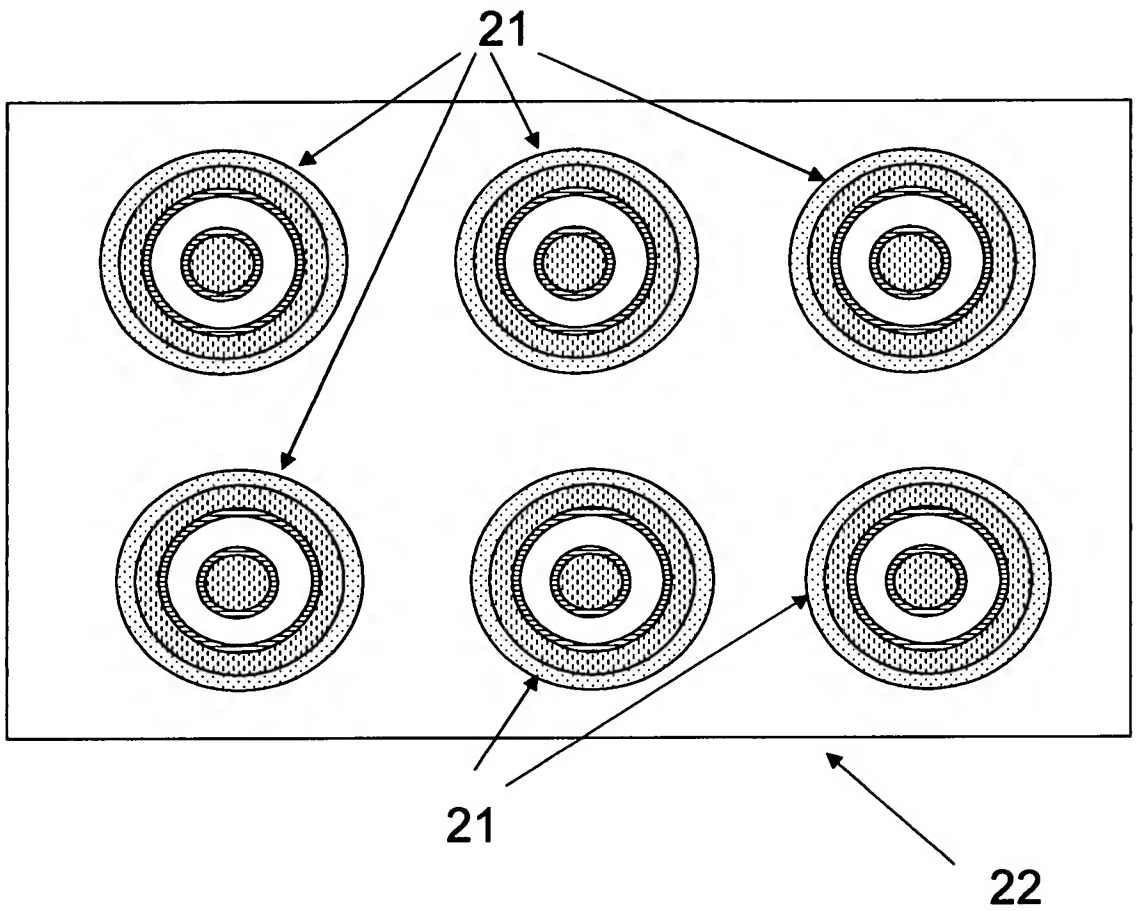

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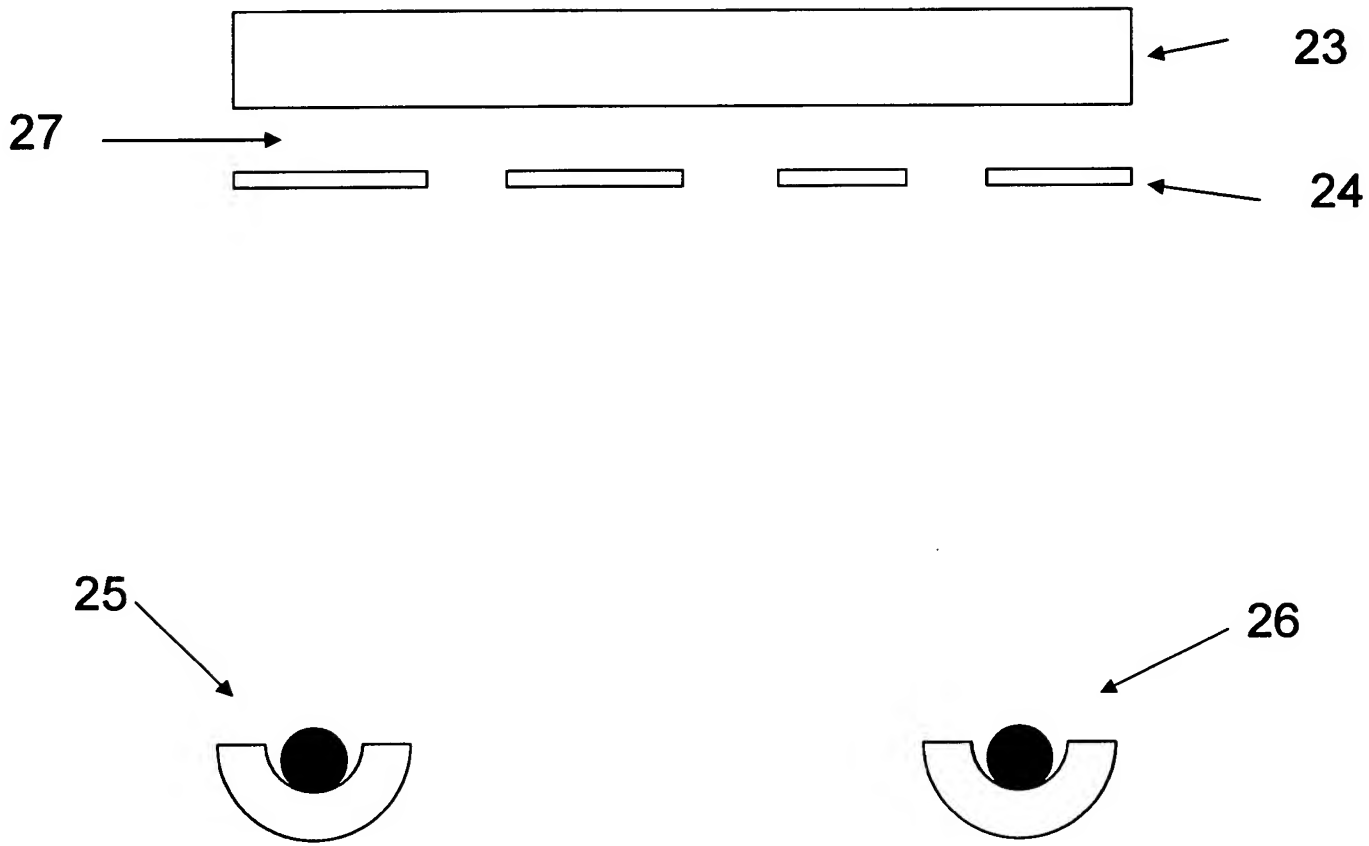

Figure 8.

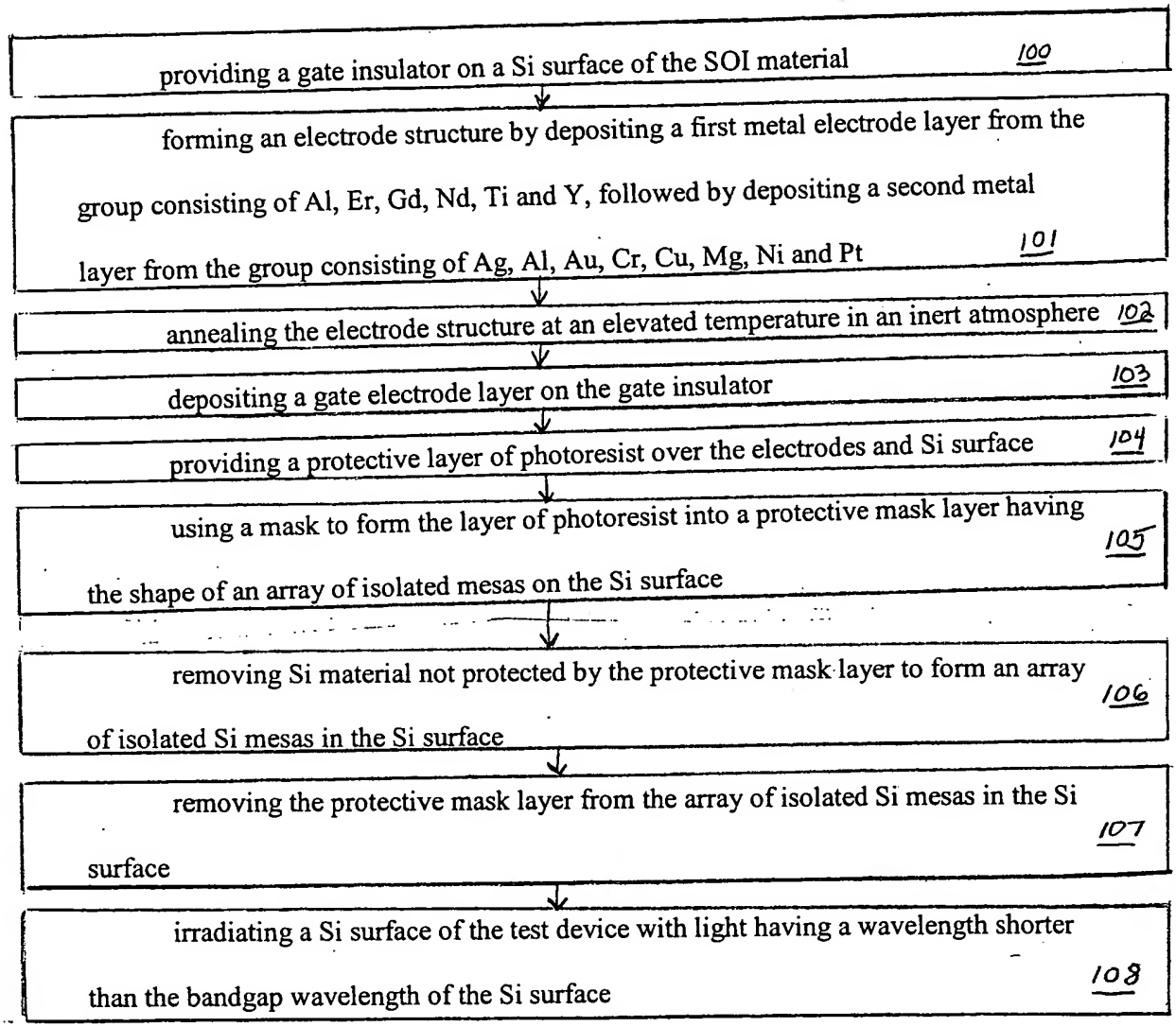
providing a gate insulator on a Si surface of the SOI material 100
forming an electrode structure by depositing a first metal electrode layer from the group consisting of Al, Er, Gd, Nd, Ti and Y, followed by depositing a second metal layer from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt 101
annealing the electrode structure at an elevated temperature in an inert atmosphere 102
depositing a gate electrode layer on the gate insulator 103
providing a protective layer of photoresist over the electrodes and Si surface 104
using a mask to form the layer of photoresist into a protective mask layer having the shape of an array of isolated mesas on the Si surface 105
removing Si material not protected by the protective mask layer to form an array of isolated Si mesas in the Si surface 106
removing the protective mask layer from the array of isolated Si mesas in the Si surface 107
irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface 108

Fig. 10

providing a gate insulator on a surface of the semiconductor layer or of the strained Si layer 110

depositing source and drain metal electrodes in a geometric pattern, including depositing a first metal electrode layer from the group consisting of Al, Er, Gd, Nd, Ti, and Y, followed by depositing a second metal layer from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni, and Pt, to form an electrode structure 111

annealing the electrode structure at an elevated temperature in an inert atmosphere 112

depositing a gate electrode on the gate insulator between the source and drain metal electrodes without contacting the source and drain metal electrodes 113

depositing a protective layer of photoresist over the entire Si surface 114

covering the protective layer of photoresist with a metal layer evaporated through a mask to form a protective mask to cover and mask the individual isolated mesas 115

creating individual isolated mesas, as an array of individual test mesa structures, of the protective layer to form a protective mask layer on the Si surface with the source, drain, and gate electrodes residing within the boundaries of the mesas; 116

removing the gate insulator and the semiconductor layers in regions between the mesas 117

removing the protective mask layer 118

irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface 119

Fig. 11

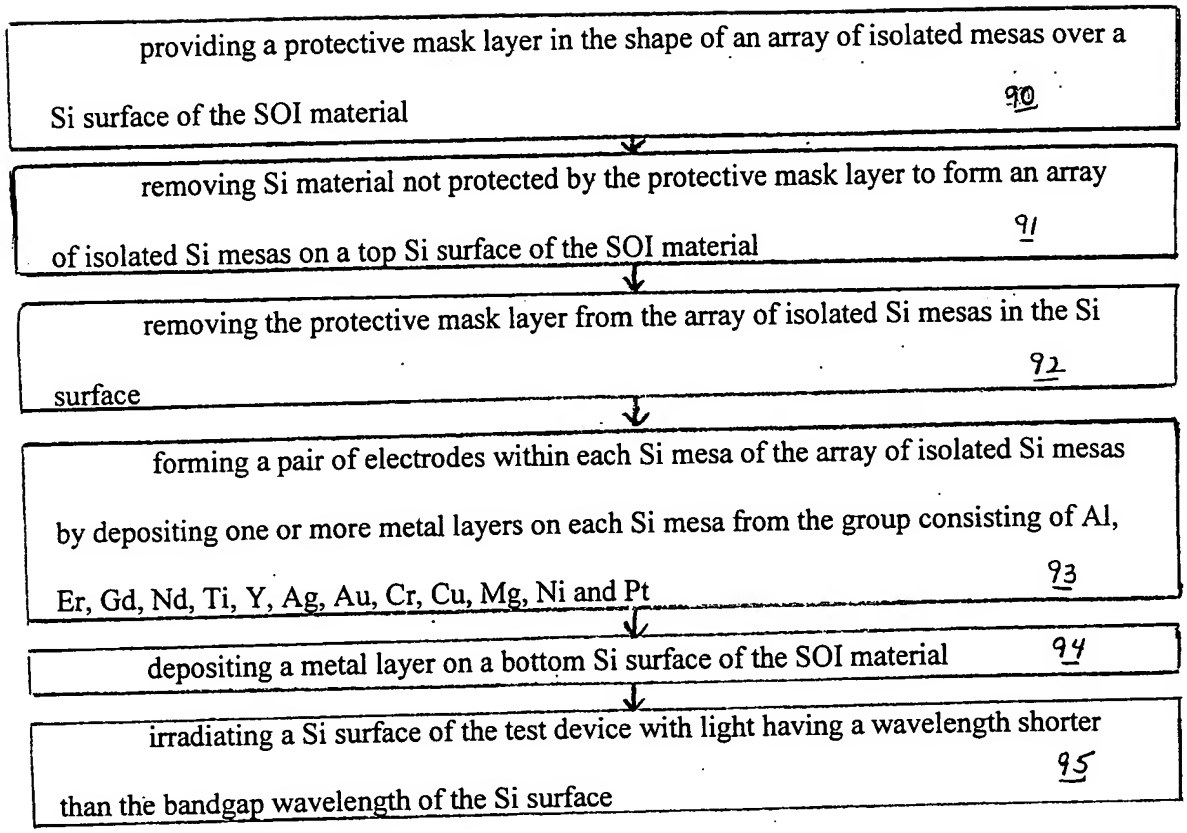
providing a protective mask layer in the shape of an array of isolated mesas over a Si surface of the SOI material
90
removing Si material not protected by the protective mask layer to form an array of isolated Si mesas on a top Si surface of the SOI material
91
removing the protective mask layer from the array of isolated Si mesas in the Si surface
92
forming a pair of electrodes within each Si mesa of the array of isolated Si mesas by depositing one or more metal layers on each Si mesa from the group consisting of Al, Er, Gd, Nd, Ti, Y, Ag, Au, Cr, Cu, Mg, Ni and Pt
93
depositing a metal layer on a bottom Si surface of the SOI material
94
irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface
95

Fig. 9

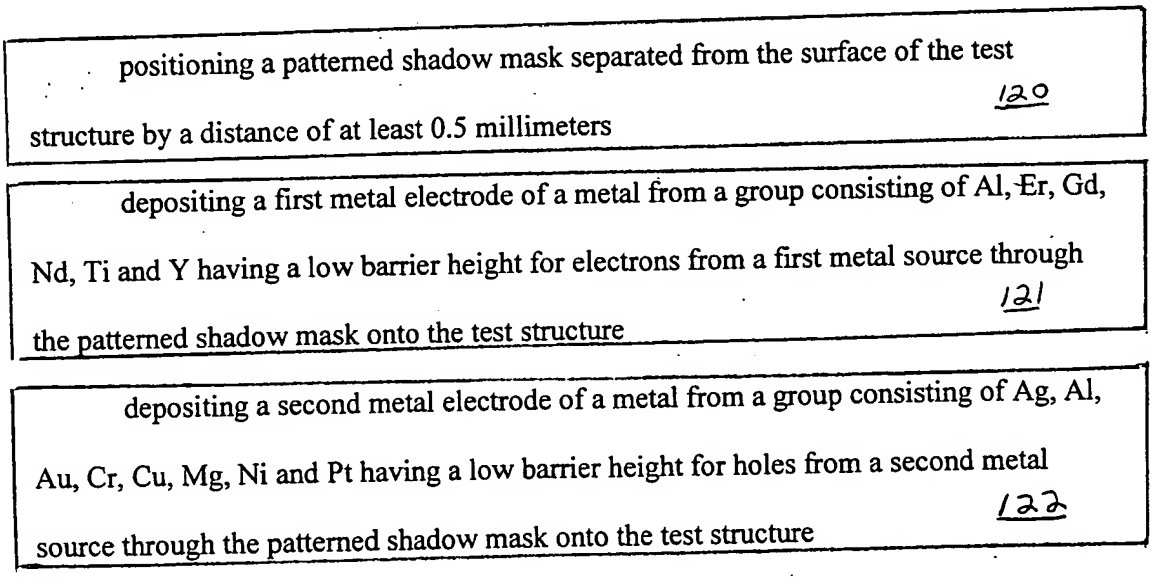
positioning a patterned shadow mask separated from the surface of the test structure by a distance of at least 0.5 millimeters
120
depositing a first metal electrode of a metal from a group consisting of Al, Er, Gd, Nd, Ti and Y having a low barrier height for electrons from a first metal source through the patterned shadow mask onto the test structure
121
depositing a second metal electrode of a metal from a group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt having a low barrier height for holes from a second metal source through the patterned shadow mask onto the test structure
122

Fig. 12